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Substitute for form 1449A/PTO		Complete if Known	
		Application Number	09/656,763
		Filing Date	September 7, 2000
		First Named Inventor	Lin Wu
		Group Art Unit	2632
		Examiner Name	Not Yet Assigned
		Attorney Docket Number	I9000.0045/P045
INFORMATION DISCLOSURE STATEMENT BY APPLICANT  <i>(use as many sheets as necessary)</i>			
Sheet	1	of	

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Examiner Signature	Date Considered	
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		Group Art Unit	2816
		Examiner Name	Not Yet Assigned
Sheet	2	of	Attorney Docket Number
		19000.0045/P045 Technology Center 2600	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Signature HAI L. NGUYEN Date Considered 6/25/01

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		Group Art Unit	2632-2816
		Examiner Name	Not Yet Assigned
Sheet	2	of	2
Attorney Docket Number I9000.0045/PG45 Technology Center 2600			

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, Application, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>HW</i>	A	T. SAEKI, et al., "A 1.3 cycle lock time, non PLL/DLL jitter suppression clock multiplier based on direct clock cycle interpolation for 'Clock on Demand'", <i>2000 IEEE International Solid-State Circuits Conference</i> (2000), p. 166-167.	
<i>HW</i>	B	I. HWANG, et al., "A digitally controlled phase-locked loop with fast locking scheme for clock synthesis application", <i>2000 IEEE International Solid-State Circuits Conference</i> (2000), p. 168-169.	

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U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

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